REMARKS

Summary of Office Action

Claims 1 and 3 stand rejected under §102(b) as allegedly being anticipated by Eto et al. (US 5,301,031), previously cited.

Claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Eto et al. in view of Sekido et al. (US 5,999,158), previously cited.

Claims 1 and 3 stand rejected under §103(a) as allegedly being unpatentable over Yamaguchi (6,329,975) in view of Eto.

Claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Yamaguchi in view of Eto et al. further in view of Sekido et al.

Claim 6 stands objected to as being dependent upon a rejected base claim, but is indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Summary of Amendment

Claims 1, 3, 4, and 6 have been amended. Claim 7 stands canceled. No new matter has been added. Claims 1-6 are pending in this application for further consideration.

Allowable Subject Matter

Claim 6 stands objected to as being dependent upon a rejected base claim, but is indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. By the amendment above, claim 6 has been rewritten in independent form incorporating all the features of its base claim 3. Accordingly, Applicant

submits that claim 6 is now in condition for allowance.

Drawing Objections

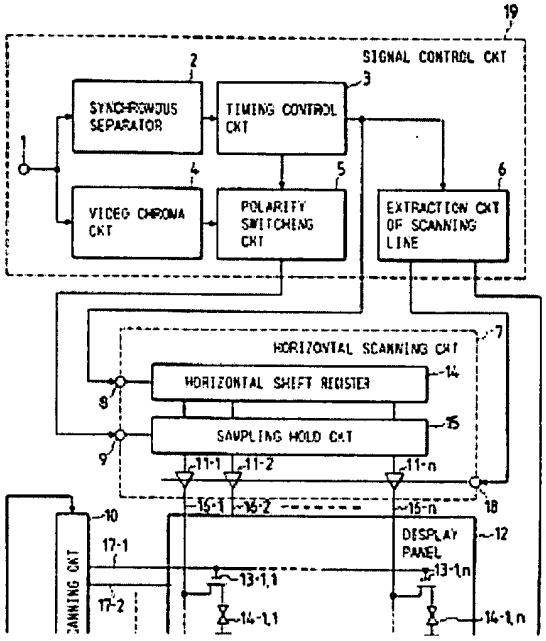
The drawings stand objected to under 37 C.F.R. §1.83(a) for allegedly failing to show every feature of the invention specified in the claims. In particular, the Office alleges that "a source shift clock reset unit" and "a reference clock generator" must be shown or the features canceled from the claims. Applicant submits that the replacement drawings filed June 20, 2006 shows all the claimed features. Moreover, the substitute specification filed June 20, 2006 describes all of the elements illustrated in the replacement drawings. Accordingly, Applicant submits that the drawings and specification are in compliance of 37 C.F.R. §1.83(a).

All Claims Comply With §102 and §103

Claims 1 and 3 stand rejected under §102(b) as allegedly being anticipated over Eto et al. Claims 1 and 3 stand rejected under §103(a) as allegedly being unpatentable over Yamaguchi in view of Eto et al. Claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Eto et al. in view of Sekido et al. Claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Yamaguchi, Eto et al. and further in view of Sekido et al. Applicant respectfully traverses for the following reasons.

As amended, independent claims 1 and 3 recite, in part, the step of receiving (claim 1) or a source shift clock reset unit (claim 3) for detecting "a data enable signal from an interface circuit being input to a timing controller." Eto et al. fails to teach at least such a feature. FIG. 1 of Eto et al. is reproduced for convenience.

FIG. 1



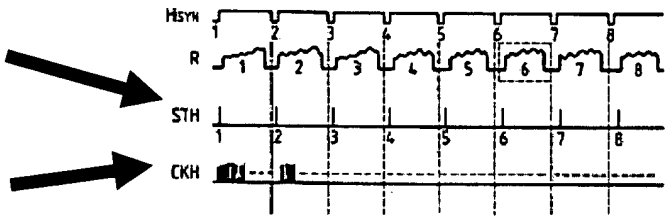
The Office alleges that the combination of circuits 2 and 3 is a "source shift clock reset unit" and circuit 14 or CKT is a "reference clock generator" for generating a source shift clock that is reset by reset signal (STH). (OA: p. 3, §3.) To the contrary, the STH signal (node 8) is not a reset signal and circuit 14 is not a source shift clock as already explained in the previous response filed January 23, 2007 and incorporated herein by reference. In addition, if, *in arguendo*, the combination of circuits 2 and 3 is considered "a source shift clock reset unit" as alleged in the Office Action, then the combination of circuits 2 and 3 (i.e., the source shift clock reset unit) cannot detect a data enable signal from an interface circuit being input to a timing controller as recited in amended claim 3 since the timing control circuit 3 is construed as part of the source shift clock reset unit. Accordingly, Eto et al. also fails to teach or suggest the step of receiving a data enable signal from an interface circuit being input to a timing controller as recited in claim

1.

Furthermore, as explained in the previous response, circuit 14 is a horizontal shift register, ***not*** a source shift clock. Additionally, the STH signal (node 8) is not a reset signal that resets the source shift clock. Rather, the STH signal is a sampling starting pulse that allows the horizontal shift register 14 to begin sampling the video signal present at node 9. (Eto: col. 4, ll. 6-10.) Accordingly, Eto et al. fails to teach or even suggest resetting a source shift clock.

In the Advisory Action, it is alleged that Eto et al. "teaches a source shift clock (14 or sampling clock) is resetting (start to generate a sampling clock signal) at the time of the reset signal pulse (STH)." As explained previously and above, circuit 14 is a shift register, ***not*** a shift clock. Accordingly, circuit 14 does not start to generate a sampling clock signal since it is not a clock circuit. Moreover, FIG. 2 of Eto et al. is reproduced and annotated below for convenience.

FIG. 2



As explained in the previous response, there is no teaching in Eto et al. that clock signal CKH is reset or "start to be generated" by the STH. Clock signal CKH is continuously generated as shown by the dotted lines. As explained in the previous response, the STH signal merely activates the shift register circuit 14 so that it starts to shift in a signal at each clock pulse (CKH) (i.e., the shift register 14 begins sampling in the video signal). There is no teaching in Eto et al.

that the clock signal CKH begins to be generated by the STH as alleged in the Office Action. Accordingly, Eto et al. fails to anticipate claims 1 and 3.

In the alternative, the Office alleges that Yamaguchi teaches resetting a source shift clock 8 using a reset signal based on a data enable signal as shown in FIG. 4 of Yamaguchi. (OA: p. 4, §5.) Applicant disagrees.

Portions of FIG. 3 and 4 of Yamaguchi are reproduced and annotated below for convenience.

FIG.3

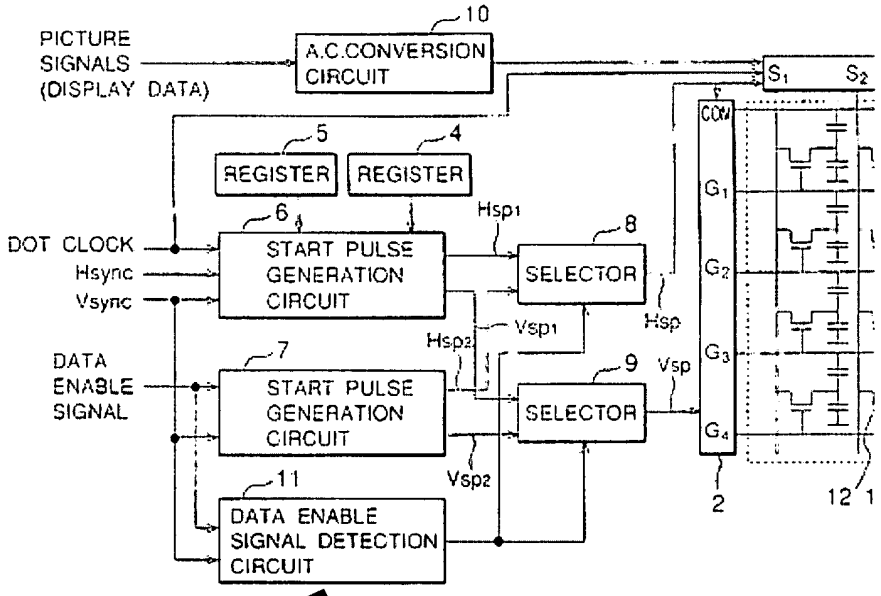
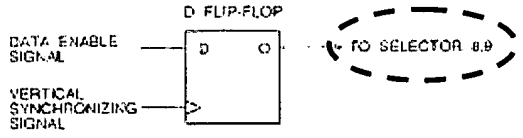


FIG.4



As explained in the previous response, incorporated herein by reference, the selector circuit 8 is ***not*** a source shift clock and the signal generated in FIG. 4 of Yamaguchi is ***not*** a reset signal that resets a source shift clock as alleged in the Office Action. Moreover, Yamaguchi fails to teach or even suggest receiving or detecting "a data enable signal from an interface circuit being input to a timing controller" as recited in amended claims 1 and 3. Accordingly, Yamaguchi and Eto et al., whether taken individually or in combination, fail to teach at least receiving or detecting "a data enable signal from an interface circuit being input to a timing controller" as recited in independent claims 1 and 3. Hence, Applicant respectfully request that the rejections to independent claims 1 and 3 be withdrawn.

Claims 2, 4, and 5 depend from and incorporates all features of corresponding one of independent claims 1 and 3 including the above features missing from Yamaguchi and Eto et al. Sekido et al. does not cure the deficiencies of Eto et al. and Yamaguchi. Therefore, Yamaguchi, Eto et al., and Sekido et al., whether taken individually or in combination, fail to teach at least the features discussed above. Hence, Applicant respectfully request that the rejections to claims 2, 4, and 5 be withdrawn.

# # # # #

CONCLUSION

In view of the foregoing, reconsideration and timely allowance of the pending claims are respectfully requested. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

By: _____
Kyle J. Choi
Reg. No. 41,480

Dated: March 5, 2007

CUSTOMER NO. 009629
MORGAN, LEWIS & BOCKIUS LLP
1111 Pennsylvania Avenue, N.W.
Washington, D.C. 20004
(202) 739-3000
(202) 739-3001